LAYOUT OPTIMIZATION OF POWER MODULES USING A SEQUENTIALLY COUPLED APPROACH

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Abstract

Nowadays, the design of Power Modules (PM) is shared between multidisciplinary teams of designers using various modelling tools. Consequently, optimizing the layout of PM is a long process with high risk of errors.

In this paper, a sequentially coupled approach is proposed to optimize this process. This integrated method is based on coupling physical models and applying an optimization process. It is illustrated through the example of the layout of a half-bridge Mosfet power module exposed to electric and thermal constraints. So, physical models and software components have been developed, in order to define the multidisciplinary design process and then to perform the layout optimization using the NLPQL algorithm.

It is shown that, the proposed approach allows automatic data exchange between physical models and optimal configurations are proposed with reduced design time and risk. Therefore, this integrated approach shows a great improvement in the design of PM and multidisciplinary products.

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Key Words: Multidisciplinary Design, Multi-Physical Coupling, Layout Optimization, Power Modules

1. INTRODUCTION

Power modules are widely used in many domains such as automotive and aircraft applications. In the design of such multidisciplinary products, layout must be optimized because it acts on both electrical and thermal performance. Layout consists in connecting semi-conductors (transistors and diodes also called chips), to external pins by using Direct Bonded Copper (DBC) tracks and wire bondings [1]. These connecting elements have electrical resistances, inductances and capacitances that can have parasitic effects on the power module. The layout has a strong effect on these parasitic elements. Thus, keeping parasitic effects low is a major requirement in order to reduce electric power losses, over-voltages and poor current balance during switching phases [2]. Long distances between chips improve the thermal dissipation of power modules, since heat spreads more easily. However, the effect of parasitic parameters increases due to the longer commutation path. Consequently, thermal dissipation contrasts with electrical performance when dealing with layout design [3]. Coupling between electric, thermal and geometric modelling is therefore necessary for optimizing power module layouts.

Today, designers are constrained to use different modelling tools in the multidisciplinary design process of power modules: mechanical design, computing parasitic elements, electrical design and finite element analysis. Exchange of data between the different modelling tools is necessary for optimizing the layout of power modules. In the classical design method,

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repeated manual data entry between the different modelling tools is performed involving errors and time consuming. Designers are often satisfied with local optimization at some modelling steps of the design process but the chosen solution may not be the global optimum.

In previous works, combined optimizing approaches were suggested [4-6]. In [4], the authors used a coupled approach to improve the thermal performance of a heat sink for integrated power modules, but without taking into account the problem of layout. In [5], the authors included parasitic capacitors and thermal effects, whereas inductance was neglected. The authors presented a numerical approach combining analytic modelling with simulation to compute thermal resistances and equivalent parasitic capacitors. In [6], the authors focused on thermal behaviour and parasitic parameters to optimize the layout of power modules. They suggested defining a grid of possible locations for the electronic components, running simulations for every location and storing results as matrices. Global optimization was performed with these matrices, but results are depending on the choice of locations.

This paper presents a systematic process to integrate multidisciplinary modelling for optimizing the layout of power modules. The different modelling tools are coupled in a Multidisciplinary Design Optimization (MDO) framework.

The first section of this paper deals with this introduction. In section 2, the method to develop the software components and the physical models, used for the integrated process, is explained. In section 3, our approach is illustrated through the example of a simple Mosfet half-bridge power module; however, the method can be generalized to any configuration. Before concluding, results of optimization process are presented and discussed in section 4.

It is shown that data exchange between software tools is automatically performed and global optimal layouts of the power module are obtained. This paper is finished with a conclusion on the great contribution of this approach for the design process of power modules and other multidisciplinary products.

2. SEQUENTIALLY COUPLED APPROACH

The approach presented is developed using the MDO framework *iSIGHT* [7]. The choice of this software is justified by its capability to be connected to a large number of various modelling tools. The integrated process is defined by connecting physical models of the power module to *iSIGHT* as illustrated in Fig. 1.
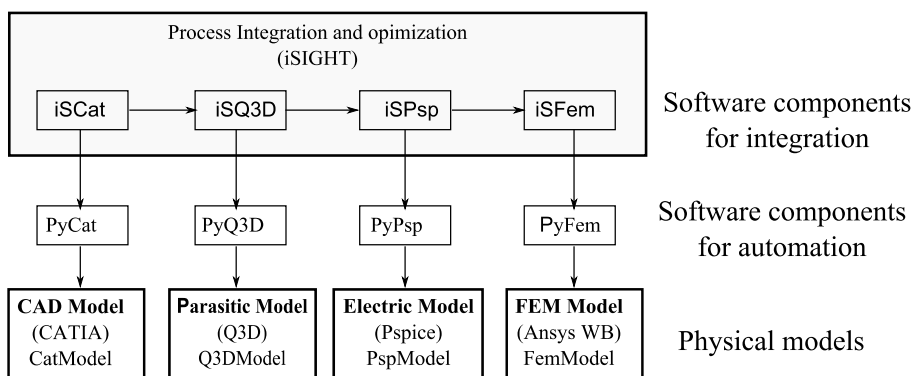

Figure 1: Illustration of the coupled approach for multidisciplinary modelling.

Some modelling tools are chosen to develop the physical models of the power module in this study. This choice is simply related to their availability, but the method can be customized for any available ones. The physical models developed are: geometric model, parasitic model, electric model and finite element model.

The 3D geometry of the power module (called *CatModel* in Fig. 1) is modelled with the CAD software *CATIA* as an assembly of parts representing the components of the power module. Geometrical parameters have to be named so that, they can be tuned in the optimization process. In practice, these parameters are chosen according to what the designer wants to optimize. They can be distances between chips, dimensions of DBC elements or a mixture of them (example in Fig. 4 of next section). Relations between dimensions are added, using the parametric modelling possibilities of *CATIA*, to keep the geometric model coherent during optimization process. Therefore, the number of failed iterations in the optimizing process is reduced. These relations are added based on geometric analysis and manual tests by tuning some parameters to see if the added relations lead usually to coherent geometrical configurations. In all cases, even if some incoherent geometrical configurations are detected during optimization process, *iSIGHT* offers the possibility to continue the process of optimization considering that the corresponding iterations have failed.

Q3D Extractor software is used to generate the parasitic model from the elements connecting semi-conductors in *CatModel* and exports them as a compact electric circuit. *Q3D Extractor* uses the Method of Moments (MoM) [8] and Finite Element Method (FEM) to solve Maxwell equations and compute parasitic element matrices. The equivalent electric circuit of the parasitic elements is exported as a *Spice Netlist* to be easily integrated in the whole electric model.

The electric model (called *PspModel*) is developed with the schematic based modelling software *Orcad/Pspice*. This model is composed of the electric model generated by *Q3D Extractor,* representing the parasitic elements, and the electric models of the semi-conductors. A finite element model (called *FemModel*) has been created using *Ansys WorkBench* (WB) software and based on *CatModel* for the thermal analysis of the power module.
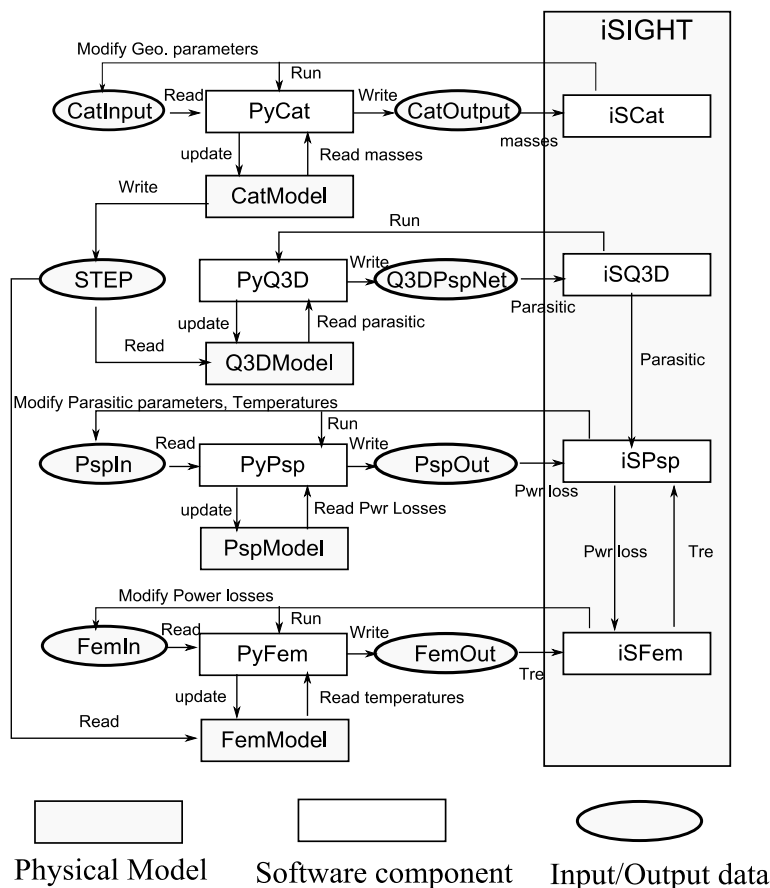

Figure 2: Coupled approach: models, software components and data exchange.

The connection between physical models and *iSIGHT* is performed using software components for automation and integration. Software components for automation are developed here for automatic update of physical models and automatic data exchange between them. Software components for integration are *iSIGHT* components developed to handle software components for automation and to manage the integrated process.

Software components for automation are developed using programming software *Python*. It is chosen in this study due to its capabilities to be connected to each of the modelling software tools via their macro − programming languages. Software components shown in Figs. 1 and 2 and labelled *PyCat*, *PyQ3D*, *PyPsp* and *PyFem* are developed to be connected to *CATIA*, *Q3D extractor*, *Orcad/Pspice* and *ANSYS WB* respectively.

When *PyCat* is executed the geometrical parameters to be optimized are read from an input text file (*CatInput*), then the geometry is updated by *CATIA*, after that the mass of elements of connection (DBC and bondings) is computed, next the mass value is saved in an output text file (*CatOutput*) and a *STEP* file is generated from the updated geometry.

PyQ3D invokes *Q3D Extractor* to run a macro (*Q3DMac*) used to automate the extraction process of parasitic elements. Therefore, the *Q3DModel* is updated with the new *STEP* file, then a parasitic model is generated and a *Pspice Netlist* (called *Q3DPspNet)* is exported.

PyPsp is used to compute the nominal electrical power losses for each transistor and saves their values in an output text file (*PspOut)*. Since power losses depends on transistor temperatures, an input text file (*PspInput)* containing temperatures is defined. *PyPsp* updates the equivalent electrical circuit of the parasitic elements in *PspModel* using the *Q3DPspNet* generated by *PyQ3D*.

PyFem updates the geometrical support of *FemModel* using the *STEP* file, reads the new values of power losses from *FemIn* and computes temperatures in transistors. These temperatures are saved in *FemOut*.

Four *iSIGHT* components are developed to handle the modelling software tools. Every *iSIGHT* component is defined by the program to run the input and output files. Therefore, *iSCat*, *iSQ3D*, *iSPsp* and *iSFem* are associated to *CATIA*, *Q3D extractor*, *Orcad/Pspice* and *Ansys WB* by means of *PyCAT*, *PyQ3D*, *PyPsp* and *PyFem* respectively.

The optimizing process is performed in the following order: firstly, *iSIGHT* runs *iSCat* which updates *CatModel* with new geometric parameters chosen by *iSIGHT,* according to an optimizing algorithm, and a new *STEP* file is generated; secondly, *iSQ3D* is executed to generate a new *Q3DPspNet*; thirdly, *iSPsp* updates *PspModel* and generates new power losses; and Finally, *iSFem* uses the new *STEP* file and the new power losses to update *FemModel* and generates new temperatures. The optimizing iterations continue until an optimum or the maximum number of iterations is reached.

3. LAYOUT OPTIMIZATION OF HALF-BRIDGE POWER MODULE

The power module investigated in this study is based on the *IXTH88N30P* Mosfet chip from *IXYS* [9]. Fig. 3 shows an electric representation and a 3D layout. Fig. 4 shows a 2D drawing of the power module and the parameters to be tuned during the optimization process. Table I gives the geometrical and physical parameters used: height h (mm), density ρ (kg/m³), heat capacity c (J/kg·K) and thermal conductivity K (W/m·K). To avoid problems of invalid geometry, relations between dimensions were defined in *CatModel*. As an example of dimensional constraints defined, the heat sink dimensions $L1$ and $L2$ was chosen to be equal to A and B respectively plus a margin that can be considered as a constant or variable parameter during optimization. In this study this margin was chosen arbitrarily constant (2.5 mm).
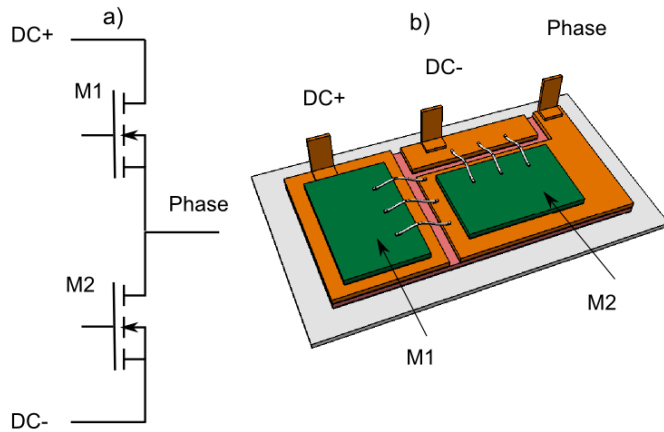
Figure 3: Power module: a) schematic; b) example of 3D layout.

1:Transistor
2:Solder
3: DBC (Copper)
4: Solder
5: Substrate (ceramic)
6: Solder
7: Heat Sink (Aluminium)
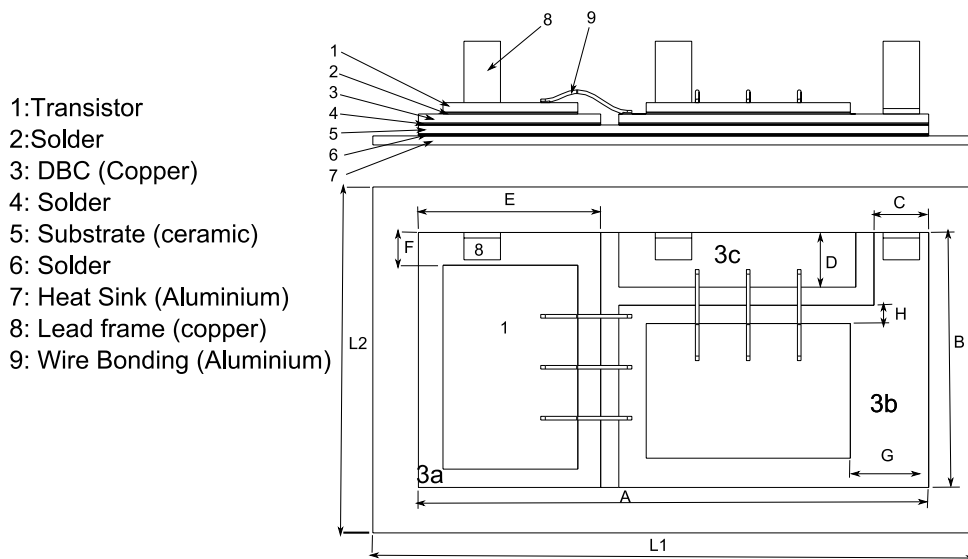8: Lead frame (copper)
9: Wire Bonding (Aluminium)

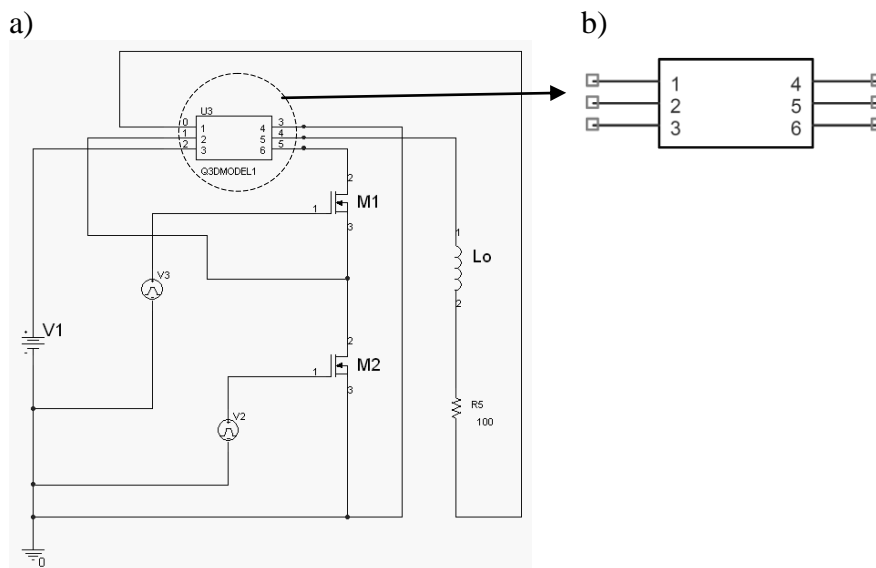Figure 4: Power module layout with changeable dimensions.

Figure 5: Electric Model: a) PspModel; b) Pspice block of equivalent parasitic elements.

Table I: Power module characteristics.

	Ref.	h (mm)	ρ (kg/m^3)	c (J/kg·K)	K (W/m·K)
Chip	1	0.525	2330	771	124
Solder	2, 4, 6	0.1	7300	180	60
Copper	3, 8	0.5, --	8900	385	390
Substrate	5	0.5	3960	880	23
Aluminium	7, 9	0.5, --	2700	897	237

The electric model equivalent to parasitic elements generated by *Q3D Extractor* (Fig. 5b) is a *Pspice* block with three input ports (1, 2 and 3) and three output ports (4, 5 and 6) associated respectively to DC-, Phase and DC+ connectors.

The electric model, shown in Fig. 5a, is created by associating the parasitic model block with the *Pspice* models of the Mosfet chips (*M1* and *M2*). During optimizing process, changes of dimensions in *CatModel* involve the parasitic model to be updated; consequently, power losses in *M1* and *M2* are also updated.

The FEM model (Fig. 6) is based on the *STEP* file generated by *PyCAT*, which is updated during optimization process, the mesh is then updated with iterations. A thermal steady state study is defined where a constant temperature T_0 is affected to the bottom face of the heat sink plate and power losses calculated previously are affected as heat flows to the top faces of the power Mosfets. During optimization iterations, the power module dimensions change but the number of faces remains the same; therefore, temperature and heat flows are always affected to the right faces.
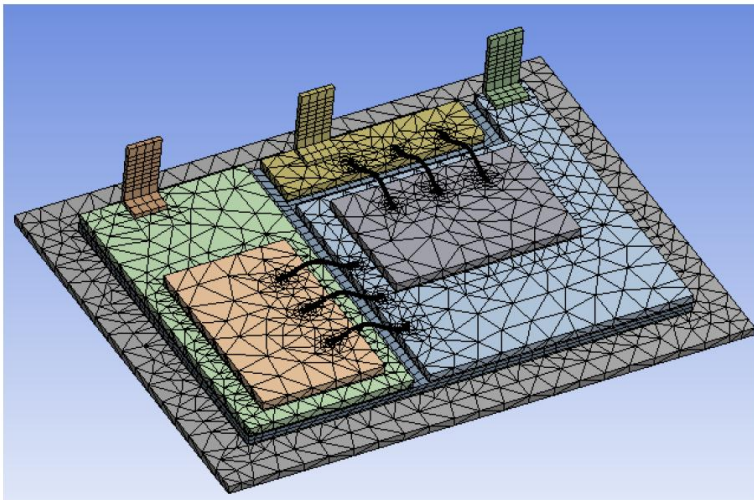

Figure 6: FEM model.

Manufacturers search usually to produce successful, but not expensive, power modules. For performance reasons temperature of Mosfets should be kept less than a limit value called junction temperature T_{jmax}. In practice this value is chosen between 140 and 160°C [9]. If T_{jmax} is reached, the power module may be deteriorated. Consequently, the temperature of Mosfets was chosen to be minimized in this study. Reducing parasitic effect is another performance indicator for power modules. Thereby, it was chosen to minimize stray inductances and stray capacitances. However, the power module studied here has three stray paths (3a, 3b, and 3c in Fig. 4); thus, three self-inductances, three mutual inductances, three self-capacitances and three mutual capacitances should be minimized. For simplification reasons only the global stray inductance and the global stray capacitance were taken into consideration. The latter two

values were calculated using Eq. (2) and (3). To reduce the cost of the power module, it was chosen to minimize the mass of connecting elements (DBC and bondings).

In this manner, to optimize the power module layout, the following objective functions were selected:

- Mass of connecting elements computed by *CATIA*.
- Global stray inductance computed by *Q3D Extractor*.
- Global stray capacitance also computed by *Q3D Extractor*.
- Mosfet temperatures computed by *Ansys Workbench*.

The multi-objective optimization problem was then formulated as:

$$\begin{cases} \min M(x_i) \\ \min L(x_i) \\ \min C(x_i) \\ \min T(x_i) \\ \text{where } T(x_i) < T_{j\,max} \\ \text{and } x_i \in [a_i \ \ b_i] \end{cases} \tag{1}$$

$M(x_i)$ is the mass (g) of connecting elements computed by *CATIA*. $L(x_i)$ is the global stray inductance (*nH*) calculated by:

$$L = \sqrt{L_1^2 + L_2^2 + L_3^2 + L_{12}^2 + L_{23}^2 + L_{13}^2} \tag{2}$$

where L_i ($i \in \{1, 2, 3\}$) are self-inductances and L_{ij} ($i, j \in \{1, 2, 3\}$) are mutual inductances.

In the same way $C(x_i)$ is the global stray capacitance (*pF*) calculated using:

$$C = \sqrt{C_1^2 + C_2^2 + C_3^2 + C_{12}^2 + C_{23}^2 + C_{13}^2} \tag{3}$$

where C_i ($i \in \{1, 2, 3\}$) are self-capacitances and C_{ij} ($i, j \in \{1, 2, 3\}$) are mutual capacitances.

$T(x_i)$ is the temperature (°C) of Mosfet computed by FEM.

$M(x_i)$, $L(x_i)$, $C(x_i)$ and $T(x_i)$ are objective functions of the optimizing problem.

x_i; ($i = 1, 2, …, N$) : design variables (geometric parameters of power module).

$[a_i \ b_i]$: Intervals of variation relative to x_i. N is the number of geometric parameters to be considered in the optimization process. In this study, parameters that have more influence on parasitic and thermal effect were chosen (parameters A, B, C, D and E in Fig. 4). In industrial cases, designers of power modules should limit the number of variables to be considered in the optimization process to reduce long computing time without influencing considerably the quality of results. The fields of variation for these parameters are chosen as following: $25 \leq A \leq 50$; $12 \leq B \leq 24$; $3 \leq C \leq 10$; $3 \leq D \leq 14$ and $7 \leq E \leq 12$. The choice of these limits depends on various constraints among them chip dimensions and the volume allocated to the power module.

The relation ($T \leq T_{jmax}$) is used as a constraint for the optimizing problem. In this study T_{jmax} was selected to be equal to 150°C.

Among the set of optimizing algorithms in *iSIGHT*, the sequential quadratic programming algorithm NLPQL [10] was chosen to solve the optimizing problem. NLPQL is a code for solving non-linear programming problems where the objective functions and constraints should be continuously differentiable. This method is based on generating a sequence of quadratic programming sub-problems obtained by a quadratic approximation of the Lagrangian function and a linearization of the constraints. This algorithm was chosen because

it is well-suited for continuous and non-linear design spaces, which is the case for the problem treated. Fig. 7 shows an example of three configurations of layout where the dimensions change during optimization process. First configuration from left notified with a), describes an initial configuration. A good choice of the initial configuration helps to converge rapidly to optimal solution. Second configuration notified with b), illustrates optimization of parameter A. Last configuration shows optimization of parameter B.

To illustrate the method, layout optimization of the half-bridge power module was achieved. Electric simulations were performed at a frequency of 250 kHz. Some simplifications were proposed to reduce the complexity of the optimizing process. Thicknesses of different power module components were chosen to be constant. Only temperature supported by Mosfet $M1$ (Fig. 3) was considered because $M1$ was connected to high-side voltage (DC+) and $M2$ to low-side. Thus, $M2$ supports low electric power dissipation. The constant temperature T_0 was chosen to be equal to 30°C.
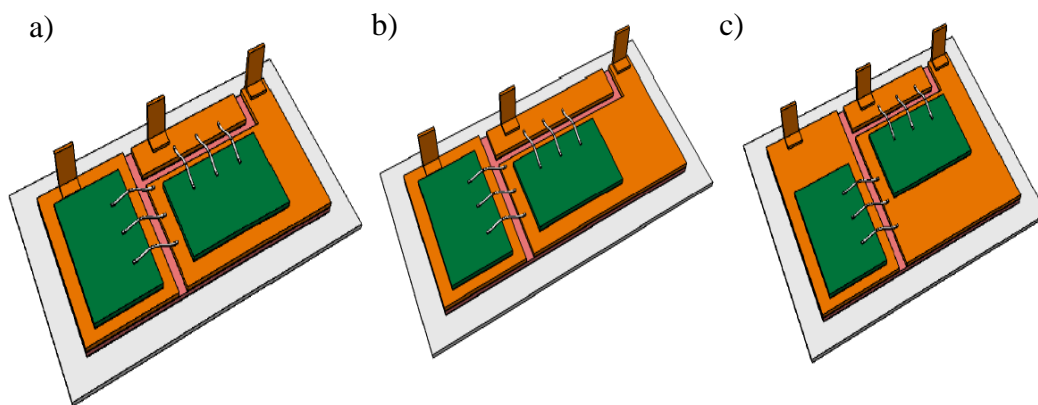
a)   b)   c)

Figure 7: Example of layout configurations: a) initial configuration, b) optimization of parameter A and c) optimization of parameter B.

4. RESULTS AND DISCUSSION

Optimization was achieved in almost 6 hours which is very short time compared to classic method of design where days are needed to reach optimal configurations. Results were sorted according to dimensions and twenty configurations were selected to be analysed (Table II, dimensions are in mm). Results of mass, inductance, capacitance and temperature are depicted in Fig. 8.

Exploring configurations from 1 to 6, where parameter A increases and other parameters are constant, results show the more the parameter A increases the more mass, inductance and capacitance increase. However, the temperature increases between configurations 1 and 2, then decreases to reach a minimum around configuration 4 and remains almost constant between configurations 5 and 6. Configuration 1 shows minimal values for mass, inductance and capacitance, but temperature is high compared to other configurations. For configurations 7 to 9, where the parameter B increases and other parameters are constant, mass, inductance and capacitance increase with B, but temperature decreases.

Configurations from 11 to 15, where parameter D is increasing, show insignificant change in mass, a little variation in capacitance and temperature; whereas, inductance increases. Configurations 18, 19 and 20 show minimal values for mass, stray inductance, stray capacitance and temperature; as a result, they are the optimal configurations.

Table II: Sorted results of optimization.

| Config.	A	B	C	D	E	Mass (g)	L (nH)	C (pF)	T (°C)
1	27	14	4	3	8	1.555	4.89	0.78	102.2
2	30	14	4	3	8	1.729	5.51	0.93	104.7
3	35	14	4	3	8	2.02	6.67	0.94	103.8
4	40	14	4	3	8	2.312	7.98	1.03	102.1
5	45	14	4	3	8	2.603	9.32	1.14	102.6
6	50	14	4	3	8	2.894	10.93	1.24	102.8
7	30	16	4	3	8	1.989	5.76	0.88	98.7
8	30	18	4	3	8	2.249	6.06	0.93	98.2
9	30	20	4	3	8	2.509	6.42	0.97	97.3
10	30	24	4	3	8	3.028	7.43	1.06	97.7
11	30	24	4	5	8	3.02	7.66	1.07	96.3
12	30	24	4	8	8	3.006	8.22	1.07	99.2
13	30	24	4	10	8	2.997	8.60	1.08	97.8
14	30	24	4	12	8	2.988	9.05	1.10	97.6
15	30	24	4	14	8	2.979	9.50	1.10	97.5
16	30	24	6	10	8	3.006	8.20	1.06	97.9
17	30	24	8	10	8	3.015	8.55	1.06	99.0
18	28	14	4	3	10	1.622	4.91	0.83	94.0
19	30	16	4	3	12	2.007	5.04	0.89	87.0
20	28	14	3	3	10	1.617	5.08	0.84	94.0

a) Mass (g)
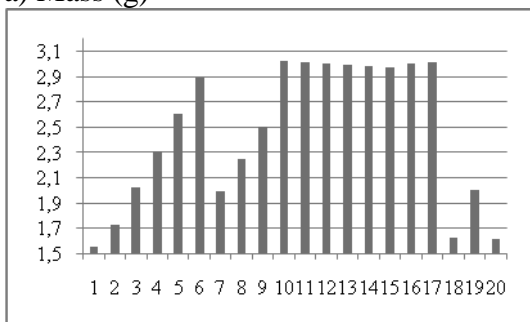
b) Inductance (nH)
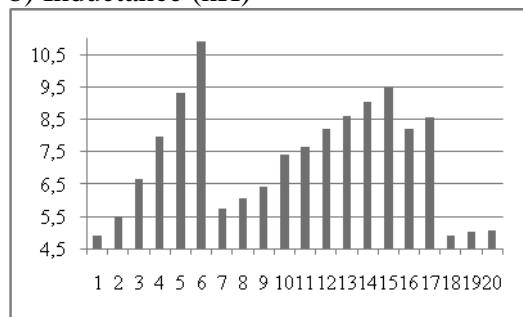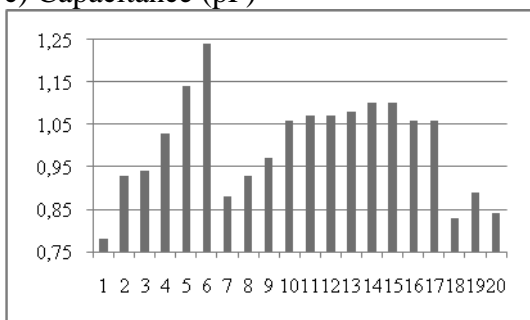
c) Capacitance (pF)
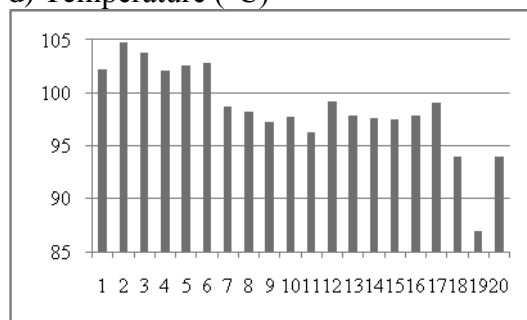
d) Temperature (°C)

Figure 8: Optimization results: a) Mass (g), b) Inductance (nH), c) Capacitance (pF) and d) Temperature (°C).

The results are coherent with those found in previous studies [3]. When the dimension *A* increases the length of the DC+ track increases; therefore, the parasitic effect increases and the temperature is reduced, around an optimal position, because the surface of heat exchange

has become larger. The same interpretation can be given for the parameter *B* which influences the length of DC- track. Results show that stray capacitance effect is more important on the DC+ track than DC-.

Since the optimization problem is multi-objective, the choice of the optimal configuration among configurations 18, 19 and 20 depends on the criterions considered most important. Therefore, configurations 18 and 20 are the optimal configurations if mass, inductance and capacitance are the retained criterions; whereas the configuration 19 is the optimal one if temperature is the chosen criterion.

Optimal configurations confirm design rules for power modules, i.e. both length of DC tracks and distances between DC+ and DC- tracks should be reduced to decrease parasitic effect. However, reducing a lot these tracks, as it has been demonstrated in is study, is antagonist with temperature.

The multi-physical aspect for optimizing the half-bridge power module was taken into account in this study. Geometric, parasitic, electric and thermal models were coupled. Manual data entry was eliminated and data exchange between physical models was automated. Global multidisciplinary optimization was performed and optimal configurations were obtained.

Designers who are familiar with the use of certain modelling tools for the design of power modules do not prefer to change them without justified arguments. The modelling tools used and physical models developed with the classical method can be used with the method proposed. Their models can be coupled by using this approach and optimization can be performed.

Some suggestions are proposed to further improve the development of the multidisciplinary optimization process. First, software components for automation and integration developed in this study should be merged so that designers will have only one component for every modelling tool which makes optimization process easier to define. Second, the step of defining input and output files for data exchange between modelling tools should be improved so that, this step becomes more simplified for the designers.

This method can have limitations, i.e. long time of computing, when dealing with design of complex power modules, since finite element models are used. However, even time of optimization is long, it is significantly reduced compared to the classical method in which optimization can last days. Another limitation to be mentioned is that the geometric topology of the power module should not change during optimization, which means that the number of faces in the geometric model should remain the same. Because if it is changed, the softwares based of the finite element method in this process (*Q3D Extractor* and *ANSYS WB*) will generate erroneous results or fail. This is due to the fact that these softwares will not be able to identify the faces on which conditions, such as flow rate, were imposed. However, this limitation concerns only cases of geometrical optimization where topology could change and this is not the case for layout optimisation where the topology does not need to be changed but only dimensions.

5. CONCLUSION

Coupling multi-physical models for layout optimization is a great need for designers of power modules. The sequentially coupled approach provided optimal layout configurations for a half-bridge power module and may be applied to other multidisciplinary products. Coupling the physical models of the power module to a multidisciplinary optimization environment and automating data exchange between them allowed us to define a multidisciplinary optimizing process to optimize the layout of power modules. The optimizing process can be limited by the cost of a long computing time when dealing with complex power modules. However, compared to classical methods, a significant reduction in optimization time was noticed.

The method of defining software components for automation of data exchange could be ameliorated to improve the process of optimization.

By its contribution in reducing the time of the design cycle and improving the design quality, the presented approach is effective and shows a significant importance in engineering design of multidisciplinary products.

<u>REFERENCES</u>

[1]   Martin, C.; Guichon, J. M.; Shannen, J. L.; Pasterczyk, R. (2006). Gate circuit layout optimization of power module regarding transient current imbalance, *IEEE Transactions on power electronics*, Vol. 21, No. 5, 1176-1184, <u>doi:10.1109/TPEL.2006.880356</u>

[2]   Martin, C.; Shannen, J. L.; Pasterczyk, R. (2004). Inside a Power Module, *39th IAS Annual Meeting, IEEE Industry Applications Conference*, Vol. 4, 1519-1525

[3]   Mühlfeld, O.; Franke, W. T.; Fuchs, F. W. (2010). Design Strategies for Stray Inductance optimized Wire-Bond Power Modules, *International Exhibition and Conference for Power Electronics, Intelligent Motion, Power Quality, PCIM 2010*, Nurenberg, Germany

[4]   Chen, J. Z.; Wu, Y.; Gence, C.; Boroyevich, D.; Bohn J. H. (2001). Integrated Electrical and Thermal Analysis of Integrated Power Electronics Modules Using iSIGHT, *Sixteenth Annual IEEE, Applied Power Electronics Conference and Exposition (APEC)*, Vol. 2, 1002-1006

[5]   Mandray, S.; Guichon, J. M.; Schanen, J. L.; Vieillard, S.; Bouzourene, A. (2009). Automatic Layout Optimization of a Double Sided Power Module Regarding Thermal and EMC constraints, *Energy Conversion Congress and Expo*, San Jose, USA, 1046-1051, <u>doi:10.1109/ECCE.2009.5316092</u>

[6]   Mühlfeld, O.; Fuchs, F. W. (2010). Comprehensive Optimization Method for Thermal Properties and Parasitics in Power Modules, *IEEE Energy Conversion Congress and Expo*, Atlanta, USA

[7]   Lee, H. J.; Lee, J. W., Lee, J. O., Development of Web services-based Multidisciplinary Design Optimization framework, *Advances in Engineering Software*, Vol. 40, No. 3, 176-183, <u>doi10.1016/j.advengsoft.2008.03.015</u>

[8]   Harrington, R. F. (1993). *Field computation by moment method*, Wiley-IEEE Press, <u>doi:10.1109/9780470544631</u>

[9]   IXYS Corporation, IXYS from *http://www.ixyspower.com/*, accessed on March 2010

[10] Schittkowski, K. (1985/86). NLPQL: A Fortran subroutine solving constrained non-linear programming problems, *Annals of Operations Research*, Vol. 5, 485-500